Schottky-Barrier Height Lowering by an Increase of the Substrate Doping in PtSi Schottky Barrier Source/Drain FETs

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***Abstract*—In this letter, the Schottky-barrier height (SBH) lowering in Pt silicide/n-Si junctions and its implications to Schottky-barrier source/drain p-field-effect transistors (p-SBFETs) are studied experimentally and numerically. We demonstrate that the increase of the n-Si substrate doping is responsible for a larger hole SBH lowering through an image-force mechanism, which leads to a substantial gain of the drive current in the long-channel bulk p-SBFETs. Numerical simulations show that the channel doping concentration is also critical for short-channel p/n-silicon-on-insulator SBFET performance.**

***Index Terms*—$PtSi_x$, Schottky-barrier (SB) lowering, Schottky-barrier source/drain field-effect transistors (SBFETs).**

I. Introduction

SCHOTTKY-barrier source/drain (S/D) field-effect transistors (SBFETs) are promising substitutes for conventional doped S/D MOSFETs for sub-22-nm CMOS technology since silicide S/D can provide abrupt junctions with low series resistance [1]–[4]. PtSi/$YbSi_{1+x}$ are considered to be among the best silicide materials for p-/n-SBFET application, but their relative low hole/electron Schottky barrier height (SBH) of $\sim$220 meV still limits drastically the drive current [2]–[4]. To make the SBFETs comparable to state-of-the-art short-channel MOSFETs in terms of drivability, the intrinsic SBH should be lowered to $\sim$100 meV [3]. Recently, it has been shown that the effective electron SBH could be lowered by inserting a thin insulator [3] or a highly doped layer (defined with a dopant segregation technique [5], [6]) at the silicide/Si junction. To our knowledge, no such method has already been reported for hole SBH. In this letter, we demonstrate experimentally and numerically that increasing the n-Si substrate doping could lower the hole SBH of PtSi/n-Si junctions through an image-force mechanism [7], which leads to a substantial gain of the drive current in the long-channel bulk p-SBFETs. Numerical simulations predict that the channel doping is also critical for short-channel silicon-on-insulator (SOI) SBFET performance improvement. SBH lowering method proposed in this letter only relies on the conventional CMOS process techniques such as well ion implantation (I/I) and is thus very promising for future SBFET development.

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II. Device Fabrication

The p-SBFETs ($W/L = 1\ \mu$m/$1\ \mu$m) were fabricated on 8-in wafers. Only the bottom part of the wafer received the well I/I: either P (3e12 cm^{-2}, 120 keV) or P (3e12 cm^{-2}, 120 keV) + As (1e12 cm^{-2}, 90 keV). In the following text, the bottom part is referred to as the south well, whereas the top part is referred to as the north well. Capacitance–voltage (C–V) measurements of MOS capacitors (data not shown) indicate a substrate doping level of 1e16 cm^{-3} in the north well and of 8e16 or 2e17 cm^{-3} in the south well, respectively, with P or P + As I/I. The gate stack is made of poly-Si and SiON, with an equivalent oxide thickness of $\sim$2 nm. Twenty-five nanometers of Pt was deposited on the substrate and thermally annealed at 550 °C (for 1 min) for the silicidation process. After a selective etching of the unreacted metal, the depth of PtSi S/D is $\sim$50 nm, as measured by cross-sectional scanning electron microscope (XSEM; data not shown). Ultraslim ($\sim$11 nm) SiN spacers were used such that S/D silicide reaches the gate edge due to a lateral diffusion of the PtSi under the spacers, which is crucial for the electrical performance improvement [8]. Note that the poly-Si electrode was activated before PtSi formation. Before the fab out of the devices, a forming gas annealing at 420 °C for 20 min was also applied.

III. Results and Discussion

A. SBH Measurement

We measured the electron SBH (ϕ_e) of PtSi/n-Si diodes fabricated on the same substrates as the SBFETs. Considering the possible high series resistance, we extracted ϕ_e from the forward current–voltage (I–V) characteristics using the Norde method [9]. A set of extracted electron SBH of PtSi/n-Si diodes is plotted in Fig. 1. SB diodes were measured in a statistical manner; i.e., they lie on a north-to-south straight line in the wafer. The electron SBH distribution of the diodes located in the north well is very tight and has an average value close to 870 meV, which is consistent with the already reported values

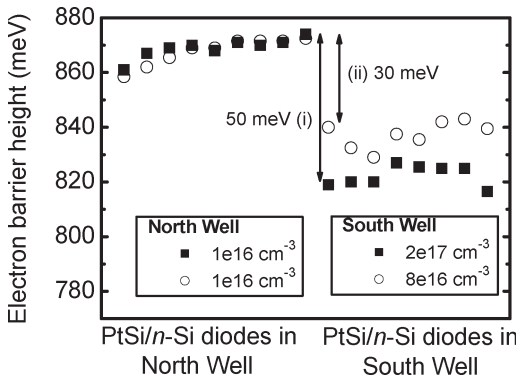

Fig. 1. Electron barrier heights extracted with Norde method of PtSi/n-Si diodes located on a straight line in the wafer. The n-type bulk Si substrate has a dopant concentration of 1e16 cm^{-3} (north well), 8e16 cm^{-3} (circle in south well), and 2e17 cm^{-3} (square in south well).

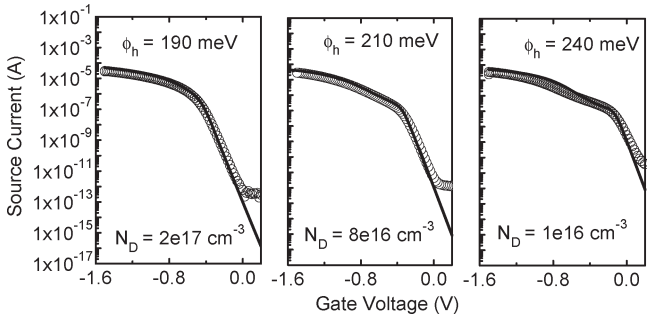

Fig. 2. Experimental (circles) and simulated (solid lines) I_s–V_g of 1-μm channel length p-SBFET with channel doping of (a) 2e17 cm^{-3}, (b) 8e16 cm^{-3}, and (c) 1e16 cm^{-3}. The hole barrier heights are 190, 210, and 240 meV, respectively, for doping concentrations of 2e17, 8e16, and 1e16 cm^{-3}. $V_d = -1.1$ V.

[1]–[3]. In the south well, the values of the SBH are a function of the doping concentration: The average value is around 840 meV for the 8e16 cm^{-3} doped substrate and 820 meV when the doping concentration is 2e17 cm^{-3}. Note that the extracted SBHs show more fluctuation in the south well. The PtSi thickness variations in the nonuniformly doped substrate are suspected to be the reason for these SBH fluctuations. It is expected that they could be minimized by improving PtSi thickness variations.

The hole SBH (ϕ_h) was extracted from a fit of previously calibrated MEDICI simulations[1] on the measured SBFET transfer characteristics. The only fitting parameter was ϕ_h; the other one was specified with the help of XSEM (not shown) and C–V measurements of the SBFETs. In Fig. 2, MEDICI simulation well matches the measured I_s–V_g of the p-SBFETs with substrate doping levels of 2e17, 8e16, and 1e16 cm^{-3}; ϕ_h is 190, 210, and 240 meV, respectively. Note that S/D junction leakage level is reduced in the highly doped transistor.

Both electron and hole SBHs are reduced by $\sim$30 and $\sim$50 meV, respectively, when the doping level rises from 1e16 to 8e16 and 2e17 cm^{-3}. This symmetrical lowering is believed

[1]MEDICI incorporates a model for calculating transport current through a Schottky contact (thermoionic and field emission) in addition to the usual MOSFET models (such as the concentration-dependant mobility). It also includes a barrier height lowering model (http://www.synopsys.com/products/tcad/taurus_medici_ds.html).

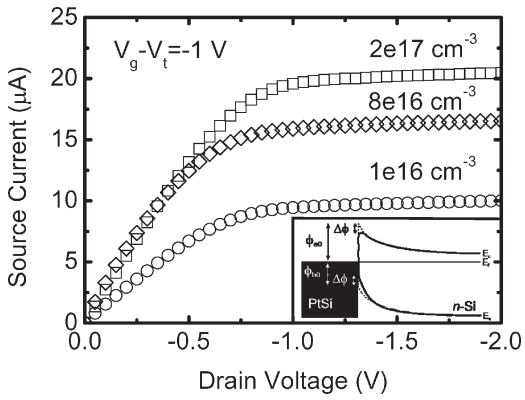

Fig. 3. Measured I_s–V_d of a 1-μm channel length SBFET on a substrate doping of 1e16 cm^{-3} (circle), 8e16 cm^{-3} (rhombus), and 2e17 cm^{-3} (square). $V_g - V_t = -1$ V. V_t is defined as the voltage corresponding to a current of 10^{-8}A. The inset shows the energy band diagram of the Pt/n-Si junction corrected by the image-force SBH lowering $\Delta\phi$ for the electron barrier height ϕ_{e0} and the hole barrier height ϕ_{h0} [7].

TABLE I
SIMULATED ELECTRIC FIELD AT THE PtSi/n-Si JUNCTION, CALCULATED ELECTRON SBH LOWERING BY [7], AND CALCULATED AND MEASURED ELECTRON SBH DIFFERENCE FROM THE 1e16 cm^{-3} DOPING LEVEL FOR DOPANT CONCENTRATIONS OF 1e16, 8e16, AND 2e17 cm^{-3}

Doping (cm^{-3})	E at interface (V/cm)	e-SBH lowering by image-force	*e*-SBH difference	
			Calculated	Measured
10^{16}	2.10^4	15.7 meV	-	-
8.10^{16}	10^5	39.3 meV	~ 25 meV	30 meV
2.10^{17}	3.10^5	60.9 meV	~ 45 meV	50 meV

to be caused by the electrostatic image force attracting the carriers to the metal and therefore reducing their energy close to the junction [7]. As sketched in the inset of Fig. 3, this results in a reduction of the electron and hole SBHs (ϕ_{e0} and ϕ_{h0}, respectively). According to the image-force lowering model ($\Delta_\phi = 2\sqrt{qE/16\pi\varepsilon_s}$) [7], we have calculated the SBH lowering from the electric field at the interface simulated in MEDICI; the data are summarized in Table I. It is shown that the simulations are in excellent agreement with our measured data, enforcing our speculation that the SBH lowering caused by the substrate doping concentration can be attributed to the image-force mechanism.

B. Performance Improvement and Extension to Short-Channel SBFETs

In Fig. 3, the measured output curves (I_s–V_d) of SBFETs (at $V_g - V_t = -1$ V) on three different substrate doping levels demonstrate the substantial gain of the drive current associated with the highest doping stemming from the SBH lowering effect. Note that even if a reduction of the hole mobility due to high substrate impurities tends to lower the drive current, the overall effect of increasing substrate doping is to enhance the drive current through the image-force barrier lowering effect.

The substrate doping concentration is also critical for the short-channel SBFET performances on SOI substrate. The MEDICI simulation of the transfer characteristics (I_s–V_g) of 100-nm channel length SBFETs on p-/n-SOI substrate with

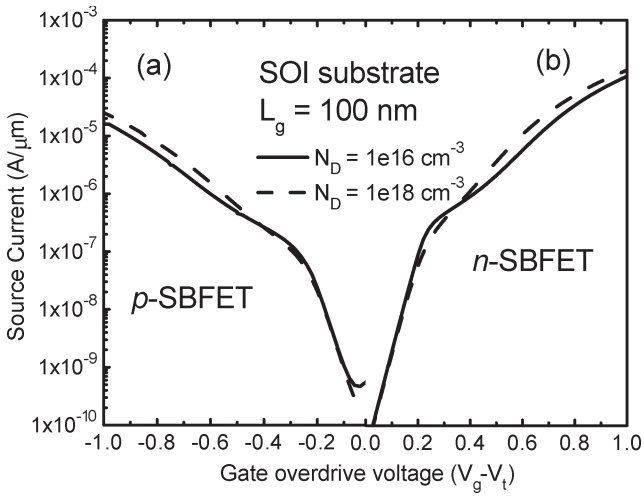

Fig. 4. Simulated transfer characteristics of a 100-nm channel length (a) PtSi and (b) $YbSi_{1+x}$ SBFET at $V_d = -1.1$ V on a SOI substrate with a Si body doping of 1e16 cm^{-3} (solid line) and 1e18 cm^{-3} (dashed line). Si body thickness is 10 nm, and silicide thickness is 4 nm.

channel doping of 1e16 and 1e18 cm^{-3} is reproduced in Fig. 4. We observe a V_t difference between both devices of $\sim$150 mV, which is inherent to the increase of the substrate doping concentration. After offsetting the V_t, it is observed that the highly doped SBFET exhibits higher drive current due to the enhanced SBH lowering. Note that the increase of V_t may be manageable by other process adjustment (such as by the tuning of the metal gate workfunction [10]).

IV. Conclusion

In conclusion, we demonstrate that hole SBH can be lowered through an image-force mechanism by increasing the n-Si substrate doping, which leads to a substantial gain of the drive current in the long-channel bulk PtSi S/D p-SBFETs. Numerical simulations show that the channel doping concentration is also beneficial for short-channel SOI n-/p-SBFETs. It would be therefore critical to adjust the well I/I for SOI SBFET to improve its performance.

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